CLAIMS

What is claimed is:

1. A nonconducting substrate forming a strip or a panel on which a plurality of carrier elements having respective boundary lines are formed, comprising:

a contact side;

an insertion side opposite the contact side; and

a conducting insertion-side metallization provided on the insertion side;

wherein the insertion-side metallization is formed such that an electrical connection can take place by means of flip-chip bonding between contact points of an integrated circuit to be applied to the insertion side and the insertion-side metallization.

2. The substrate according to Claim 1, further comprising a plurality of contact elements provided on the insertion-side metallization within each boundary line at least partly for bonding with flip-chip contacts of the integrated circuit.

3. The substrate according to Claim 1, further comprising a contact-side metallization provided on the contact side of the substrate.

4. The substrate according to Claim 3, further comprising a plurality of contact areas which are electrically isolated from one another and are provided on the contact-side metallization within each boundary line.

5. The substrate according to Claim 4, wherein the contact areas of the contact-side metallization are formed as ISO contact areas.

6. The substrate according to Claim 4, further comprising:

a plurality of contact elements provided on the insertion-side metallization within each boundary line at least partly for bonding with flip-chip contacts of the integrated circuit,

wherein the contact areas of the contact-side metallization have at least partly an electrical connection with the contact elements of the insertion-side metallization.

7. The substrate according to Claim 6, wherein the electrical connection is established by plated-through holes extending through the substrate.

8. The substrate according to Claim 7, wherein the plated-through holes are each arranged in a plated-through region of the contact areas of the contact-side metallization which is not intended for bonding with an external reader (ISO zone).

9. The substrate according to Claim 3, further comprising a boundary line region which includes the contact-side metallization and brings about an increased moment of resistance in a region of the integrated circuit.

10. The substrate according to Claim 9, wherein the boundary line region crosses a line of symmetry, which is formed between oppositely lying contact areas of the contact-side metallization.

11. The substrate according to Claim 2, wherein the contact elements of the insertion-side metallization are in a form of interconnects, which respectively have a first end and a second end.

12. The substrate according to Claim 7, wherein the contact elements of the insertion-side metallization are in a form of interconnects, which respectively have a first end and a second end, the first end of the interconnects overlapping with a respective one of the plated-through holes and being in electrical connection therewith.

13. The substrate according to Claim 11, wherein the second end has a first contact area for the electrical bonding with a flip-chip contact of the integrated circuit.

14. The substrate according to Claim 13, wherein at least some of the interconnects have at least a further contact area, which is in electrical contact with the first contact area of the interconnect either directly or via a portion of the interconnect connected to the first contact area, the respective further contact areas being provided for the electrical bonding with a flip-chip contact of the integrated circuit.

15. The substrate according to Claim 11, wherein at least some of the interconnects have at least a further contact area, which is in electrical contact with the interconnect via an interconnect branch, the respective further contact areas being provided for the electrical bonding with a flip-chip contact of the integrated circuit.

16. The substrate according to Claim 14, wherein the contact areas and the further contact areas serve as control marks when the integrated circuit is applied, in that the contact areas protrude slightly beyond side edges of the integrated circuit.

17. The substrate according to Claim 15, wherein the contact areas and the further contact areas serve as control marks when the integrated circuit is applied, in that the contact areas protrude slightly beyond side edges of the integrated circuit.

18. The substrate according to Claim 11, wherein at least some of the interconnects are provided with area-covering metallizations, which serve for increasing the bending rigidity of the substrate.

19. The substrate according to Claim 18, wherein the area-covering metallizations are formed within the boundary line of the respective carrier element.

20. The substrate according to Claim 18, wherein the area-covering metallizations are provided in a region outside the integrated circuit to be applied.

21. The substrate according to Claim 1, further comprising indexing holes, which are provided on the substrate, and to stiffen the substrate, are surrounded by metallizations on the insertion side and/or the contact side.

22. The substrate according to Claim 3, further comprising adjusting marks which constitute part of the insertion-side metallization and/or the contact-side metallization and are provided on the substrate for orientation of placement machines.

23. The substrate according to Claim 3, further comprising transverse webs which constitute part of the insertion-side metallization and/or contact-side metallization and are provided on the substrate between neighbouring carrier elements.

24. The substrate according to Claim 1, wherein, in a region of the integrated circuit to be applied, the insertion-side metallization comprises spacers which ensure plane-parallelism between the integrated circuit and the insertion side of the substrate.

25. The substrate according to Claim 1, further comprising a stiffening frame arranged on the insertion side of the substrate and surrounding a region intended for the integrated circuit to be applied.

26. The substrate according to Claim 25, wherein the stiffening frame is part of the insertion-side metallization.

27. The substrate according to Claim 25, wherein the stiffening frame has, in a region where it crosses or overlaps with contact elements of the insertion-side metallization, interruptions in order to avoid short-circuits.

28. The substrate according to Claim 26, wherein the stiffening frame consists of a nonconducting material.

29. The substrate according to Claim 28, wherein the stiffening frame completely surrounds the region intended for the integrated circuit to be applied.

30. The substrate according to Claim 1, wherein the substrate consists of at least one of PEN, PET, PI, and paper.

31. The substrate according to Claim 30, wherein the thickness of the substrate is approximately 50 to 125 μm.

32. The substrate according to Claim 3, wherein the contact-side metallization and the insertion-side metallization are produced by a growing-on process.

33. The substrate according to Claim 32, wherein the contact-side metallization and the insertion-side metallization have a thickness of less than 40 μm.